UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,233	11/26/2001	Michael A. Nix	X-1012 US	8295

24309 7590 10/04/2002

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
NGUYEN, LONG T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/994,233	NIX, MICHAEL A.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 5, 9, 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is indefinite because the recitation "the second control terminal" on the last line of the claim lacks antecedent basis. It appears that claim 4 should be depended on claim 3.

Claim 5 is indefinite because it includes the indefiniteness of claim 4.

Claim 9 is indefinite because the recitation "the first and second clock terminals" on lines 1-2 lacks antecedent basis.

Claim 11 is indefinite because the recitation "the first transistor having a first control terminal connected to the first input terminal and a second control terminal connected to the third input terminal" on lines 3-6 is misdescriptive. Figure 6 of the invention shows a first leg (605) including first and second transistors (620 and 615) connected in parallel, the first transistor (620) having a first control terminal (gate) connected to the first input terminal (D0) and the second transistor (615) having a second control terminal (gate) connected to the third input terminal (D1), not the first transistor having a first control terminal connected to the first input terminal and a second control terminal connected to the third input terminal. It is suggested that "the first transistor having a first control terminal connected to the first input terminal and a second control terminal connected to the third input terminal" on lines 3-6 be changed to --the

first transistor having a first control terminal connected to the first input terminal and the second transistor having a second control terminal connected to the third input terminal--.

Claim 12 is indefinite because it includes the indefiniteness of claim 11.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (JP 2000244287).

With respect to claim 1, Figure 9 of the Ooishi reference discloses a flip-flop circuit which includes: a differential output stage (23-24) having differential first and second input terminals (D3 and /D3) and complementary first and second output terminals (nodes OD4 and OD3); and a transistor (NT3) having a first current-handling terminal connected to the first output terminal (OD4), a second current-handling terminal connected to the second output terminal (OD3), and a control terminal (gate).

With respect to claim 2, Figure 9 shows a clock terminal (TG2) connected to the control terminal (gate of transistor NT3 connected to receiving clock TG2).

With respect to claim 3, Figure 9 shows a second transistor (n-channel transistor of transmission gate CQ1) having a third current-handling terminal connected to the first input terminal (D3), a fourth current-handling terminal connected to the second input terminal (/D3), and a second control terminal (gate).

With respect to claim 4, Figure 9 of the Ooishi reference includes a first clock terminal (TG2) connected to the first-mentioned control terminal (gate of transistor NT3 connected to receive clock signal TG2) and a second clock terminal (TG1) connected to the second control terminal (gate of n-channel transistor of transmission gate CQ1 connected to receive clock TG1). Note that the Examiner treats this claim as if it depends on claim 3.

With respect to claim 5, the limitation "the first and second clock terminals are adapted to receive complementary clock signals" is met because clocks TG2 and TG1 are complementary clock signals (see Figure 10).

With respect to claim 6, Figure 9 of the Ooishi reference shows that the flip-flop circuit includes a differential input stage (21-22) having differential third and fourth input terminals (D and /D) and complementary third and fourth output terminals (nodes OD2 and OD1) connected to the first and second input terminals (D3 and D3/), respectively.

With respect to claim 7, Figure 9 shows a clock terminal (TG2) connected to the control terminal (gate of transistor NT3 connected to receive clock signal TG2).

With respect to claim 8, Figure 9 shows a second transistor (n-channel transistor of transmission gate CQ1) having a third current-handling terminal connected to the first input terminal (D3), a fourth current-handling terminal connected to the second input terminal (/D3), and a second control terminal (gate of n-channel transistor of transmission gate CQ1).

With respect to claim 9, Figure 9 shows a second clock terminal (TG1) connected to the second control terminal (gate of the n-channel transistor of transmission gate CQ1), and the clock terminal (TG2) and the second clock terminal (TG1) are adapted to receive complementary clock signals (TG2 and TG1 are complementary clock signals, see Figure 10).

5. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Rollins et al. (USP 5,036,217).

With respect to claim 10, Figure 3B of the Rollins et al. reference discloses a flip-flop circuit 600 (Col. 4, lines 44-47) which includes a differential input stage (the combination of transistors 602, 604, 606, 608, 610, 612, 614, 616 and 618) having differential first and second input terminals (gate of transistors 614 and 612 which receive Q0 and Q0', respectively), differential third and fourth input terminals (gate of transistors 616 and 608 which receive MOD and MOD', respectively), and complementary first and second output terminals (631 and 633).

Insofar as understood in claim 11, Figure 3B of the Rollins et al. reference shows that the input stage (the combination of transistors 602, 604, 606, 608, 610, 612, 614, 616 and 618) includes a first leg (transistors 614 and 616) having first and second transistors (614 and 616) connected in parallel, the first transistor (614) having a first control terminal (gate) connected to the first input terminal (gate of transistor 614 connected to receive signal Q0) and the second transistor (616) having a second control terminal (gate) connected to the third input terminal (gate of transistor 616 connected to receive signal Q0).

With respect to claim 12, Figure 3B of the Rollins et al. reference shows that the input stage (the combination of transistors 602, 604, 606, 608, 610, 612, 614, 616 and 618) includes a second leg (transistors 612 and 608) having third and fourth transistors (612 and 608) connected in series, the third transistor (612) having a third control signal (gate) connected to the second input terminal (gate of transistor 612 connected to receive signal Q0') and the fourth transistor (608) having a fourth control terminal (gate) connected to the fourth input terminal (gate of transistor 608 connected to receive signal MOD').

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rollins et al. (USP 5,036,217) in view of Choe (USP 6,373,292).

With respect to claim 13, Figure 3B of the Rollins et al. reference discloses a flip-flop circuit 600 (Col. 4, lines 44-47) which includes all of the limitations of this claim except for the limitation that the differential input stage of the flip-flop circuit includes a transistor having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal. However, Figure 2 of the Choe reference discloses a differential circuit which includes a transistor (56) having a control terminal (gate), a first current-handling terminal connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of reducing power consumption and improving the speed of the circuitry (line 25 of Col. 2 to line 10 of Col. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the differential stages (601 and 619) in the flip-flop circuit 600 (Figure 3B) of the Rollins et al. reference with a transistor connected between the outputs of each differential stage (i.e., a transistor connected between nodes 631 and 633 in the differential stage 601, and also another transistor connected between the output nodes Q0 and

Q0' in the differential stage 619), as taught by the Choe reference, for the purpose of reducing power consumption and improving the speed of the circuitry.

With respect to claim 14, the above combination meets the limitation of a clock terminal connected to the control terminal (i.e., a clock signal is connected the gate of the transistor that has the first and second current-handling terminals connected to nodes 631 and 633, respectively).

With respect to claim 15, the above combination includes an output stage (619) having: differential fifth and sixth input terminals (gate of transistors 622 and 624) connected to respective ones of the first and second output terminals (nodes 631 and 633); complementary third and fourth output terminals (terminals provides outputs Q0 and Q0' in the output stage 619); and a transistor (as discussed above with regard to claim 13) having a control terminal (gate), a first current-handling terminal connected to the third output terminal (the terminal which provides output Q0) and a second current-handling terminal connected to the fourth output terminal (the terminal which provides output Q0').

With respect to claim 16, the above combination also meets the limitation of a clock terminal connected to the control terminal (i.e., a clock signal is connected to the gate of the transistor that has the first and second current-handling terminals connected to outputs Q0 and Q0', respectively).

8. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (Figure 1) in view of Ooishi (JP 2000244287).

Applicant's admitted prior art (Figure 1) discloses a counter circuit which includes a first flip-flop (first flip-flop 110 from the left) having differential first and second outputs (Q and Q/

of the first flip-flop) and a second flip-flop (second flip-flop 110 from the left) having differential first and second inputs (D and D/ of the second flip-flop) wherein the differential first and second inputs of the second flip-flop are connected to receive the differential first and second outputs of the first flip-flop, respectively, wherein the details of each flip-flop 110 in Figure 1 are shown in instant Figure 2 (prior art). Applicant's admitted prior art does not disclose that the flip-flop includes a differential output stage having differential first and second input terminals, complementary first and second output terminals, and a first transistor having a first control terminal, a first current-handling terminal connected to the first output terminal and a second current-handling terminal connected to the second output terminal; and the second flip-flop includes a differential input stage having differential third and fourth input terminals, complementary third and fourth output terminals, and a second transistor having a second control terminal and third and fourth current-handling terminals connected to the third and fourth output terminals, respectively. However, Figure 9 of the Ooishi reference discloses a flip-flop circuit which operates at high-speed and low current consumption (see Col. 17, lines 42-57 of US Patent 6,433,586 which is the English version of the JP 2000244287 reference) which includes: a differential output stage (23-25) having differential first and second input terminals (D3 and /D3) and complementary first and second output terminals (OQ and /OQ), and a first transistor (NT3) having a first control terminal (gate of NT3), a first current-handling terminal connected to the first output terminal (OQ by way of inverter 25a) and a second current-handling terminal connected to the second output terminal (/OQ by way of inverter 25b); and a differential input stage (21-22) having differential third and fourth input terminals (D and /D) and complementary third and fourth output terminals (nodes OD2 and OD1) connected to the first and second input

terminals (D3 and D3/) of the differential output stage, respectively, and a second transistor (the n-channel transistor of transmission gate CQ1) having a second control terminal (gate) and third and fourth current-handling terminals connected to the third and fourth output terminals (nodes OD2 and OD1), respectively. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace each of flip-flops 110 in Figure 1 of applicant's admitted prior art (the details of each flip-flop are shown in Figure 2) with the flip-flop shown in Figure 9 of the Ooishi reference for the purpose of reducing the current consumption of the circuitry and operating the circuitry at high-speed. Thus, based on this combination, the limitations recited claim 17 are met.

With respect to claim 18, the above combination meets the limitation "the first and second control terminals are adapted to receive complementary clock signals" recited in this claim because clocks signals TG2 and TG1 are complementary clock signals (see Figure 10).

With respect to claim 19, the first flip-flop (the first flip-flop from the left in the above combination) includes a second differential input stage (i.e., 21-22 in Figure 9 of the Ooishi reference) having differential fifth and sixth input terminals (D and D/ in Figure 9 of the Ooishi reference) and complementary fifth and sixth output terminals (nodes OD2 and OD1 in Figure 9 of the Ooishi reference), wherein the fifth and sixth output terminals (nodes OD2 and OD1) are connected to the first and second input terminals (D3 and /D3), respectively.

With respect to claim 20, the second flip-flop (the second flip-flop from the left in the above combination) includes a second differential output stage (23-25 in Figure 9 of the Ooishi reference) having differential fifth and sixth input terminals (D3 and /D3 in Figure 9) connected to the third and fourth output terminals (nodes OD2 and OD1 in Figure 9), respectively.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

September 30, 2002

Long Nguyen
Art Unit: 2816